Notice of Allowability	Application No.	Applicant(s)	
	09/347,690	KHAIRA ET AL.	
	Examiner	Art Unit	
	Dwin M. Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/23/06*.

2. ☒ The allowed claim(s) is/are *4-9,12,13,15,19,20 and 24-27*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

And

EXAMINER'S REASONS FOR ALLOWANCE

1. Claims 4-9, 12, 13, 15, 19, 20, 24, 25, 26 and 27 are allowed.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mark V. Muller Reg. No. 37,509 on 28 August 2006.

The application has been amended as follows:

The word "and" in line 8 of claim 4 has been deleted.

Claim 4 line 9 has been changed from "seeds." to -- seeds; loading the decomposed circuit model into memory. --.

The word "and" in line 4 of claim 5 has been deleted.

Claim 5 line 9 has been changed from "cells." to -- cells; loading the decomposed circuit model into memory. --.

Claim 5 line 7 has been changed from "of extend latch" to -- of extended latch --.

The word "and" in line 4 of claim 7 has been deleted.

Claim 7 line 9 has been changed from "size." to -- size; loading the decomposed circuit model into memory. --.

The word "and" in line 4 of claim 9 has been deleted.

Claim 9 line 9 has bee changed from "balancing." to -- balancing; loading the decomposed circuit model into memory. --.

The word "and" in line 6 of claim 12 has been deleted.

Claim 12 line 8 has been changed from "about 110% of" to -- about 120% of --.

Claim 12 line 9 has been changed from "size." to -- size; loading the plurality of partitions into memory. --.

Claim 13 line 2 has been changed from "about 120% of" to -- about 110% of --.

The word "and" in line 6 of claim 15 has been deleted.

Claim 15 line 8 has been changed from "grouping." to -- grouping; loading the plurality of partitions into memory. --.

The word "and" in line 4 of claim 19 has been deleted.

Claim 19 line 8 has been changed from "circuit model." to -- circuit model; loading the expanded circuit structure into memory. --.

The word "and" in line 4 of claim 20 has been deleted.

Claim 20 line 8 has been changed from "circuit structure." to -- circuit structure; loading the expanded circuit structure into memory. --.

Examiner's reasons for allowance

3. The following is an examiner's statement of reasons for allowance:

3.1 As regards independent claim 4, while *Manjikian* discloses partitioning of boundary latches and *Panderson* discloses bin-packing heuristics, none of these references taken alone or in combination with the prior art of record disclose, constructing a plurality of seeds and merging the boundary latch components with the plurality of seeds, specifically including:

(claim 4) "...wherein using the bin-packing heuristic comprises: constructing a plurality of seeds from the plurality of extended latch boundary components; merging the plurality of extended latch boundary components with the plurality of seeds;...", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art.

3.2 As regards independent claim 5, while *Manjikian* discloses partitioning of boundary latches and *Panderson* discloses bin-packing heuristics, none of these references taken alone or in combination with the prior art of record disclose, identifying an extended latch boundary component that meets a size constraint, specifically including:

(claim 5) "...wherein decomposing the circuit model having a number of latches into a plurality of extended latch boundary components comprises: identifying an extended latch boundary component that meets a size constraint for at least one of a plurality of hierarchical cells;...", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art.

3.3 As regards independent claim 7, while *Manjikian* discloses partitioning of boundary latches and *Panderson* discloses bin-packing heuristics, none of these references taken alone or in combination with the prior art of record disclose, grouping the plurality of extended latch boundary components to form a plurality of partitions, specifically including:

(claim 7) "...grouping the plurality of extended latch boundary components to form a plurality of partitions, each of the plurality of partitions having a size...", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art.

3.4 As regards independent claim 9, while *Manjikian* discloses partitioning of boundary latches and *Panderson* discloses bin-packing heuristics, none of these references taken alone or in combination with the prior art of record disclose, partitioning the latch boundary groups based on activity, specifically including:

(claim 9) "...partitioning the plurality of extended latch boundary components based on activity load balancing...", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art.

3.5 As regards independent claim 12, while *Manjikian* discloses partitioning of boundary latches and *Panderson* discloses bin-packing heuristics, none of these references taken alone or in combination with the prior art of record disclose, adjusting the load balance to obtain a partition size of less than 120% of the model size, specifically including:

(claim 12) "...adjusting the load balance to obtain a partition size of less than 120% of the model size;...", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art.

3.6 As regards independent claim 15, while *Manjikian* discloses partitioning of boundary latches and *Panderson* discloses bin-packing heuristics, none of these references taken alone or in combination with the prior art of record disclose, reducing the communication time within the plurality of partitions to less than about ten percent of the total simulation time by adjusting the grouping, specifically including:

(claim 15) "...reducing the communication time within the plurality of partitions to less than about ten percent of the total simulation time by adjusting the grouping;..." , in combination

with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art.

3.7 As regards independent claim 19, while *Manjikian* discloses partitioning of boundary latches and *Panderson* discloses bin-packing heuristics, none of these references taken alone or in combination with the prior art of record disclose, copying a table representing the circuit model to add expanded circuit structure, specifically including:

(claim 19) "...wherein grafting the expanded circuit structure to the circuit model as needed comprises: copying a table representing the circuit model to add expanded circuit structure;...", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art.

3.8 As regards independent claim 20, while *Manjikian* discloses partitioning of boundary latches and *Panderson* discloses bin-packing heuristics, none of these references taken alone or in combination with the prior art of record disclose, altering a table representing the circuit model, specifically including:

(claim 20) "...wherein grafting the expanded circuit structure to the circuit model as needed comprises: altering a table representing the circuit model to add the expanded circuit structure;...", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art.

3.9 As regards independent claim 24, while *Manjikian* discloses partitioning of boundary latches and *Panderson* discloses bin-packing heuristics, none of these references taken alone or in combination with the prior art of record disclose, a dicing unit capable of decomposing a circuit model into a plurality of extended latch components, specifically including:

(claim 24) "...a dicing unit operably coupled to the processor unit, capable of executing on the processing unit, and capable of decomposing a circuit model into a plurality of extended latch boundary components, and capable of partitioning the plurality of extended latch boundary components;...", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art.

3.10 As regards dependent claims 6, 8, 13 and 25-27 they are allowed for at least the reason that they depend upon an allowed base claim.

3.11 Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M. Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dwin McTaggart Craig

8/30/06

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